ABSTRACT OF THE DISCLOSURE

A data detection circuit includes a transient detector that senses transient events in data. A first data detector path applies a first equalization target to generate a first bit stream from the data. A second data detector path applies a second equalization target to generate a second bit stream from the data. A baseline correction circuit generates a baseline correction signal using the first bit stream when the transient detector does not sense the transient events and the second bit stream when the transient detector senses the transient events. The first equalization target is a non-DC free equalization target and the second equalization target is a DC-free equalization target. When transients are detected during a sector, the detection circuit continues using the DC-free equalization target until the sector ends.